REMARKS

The claims are claims 1 to 4, 16, 17 and 27 to 36.

The application has been amended at many locations to correct minor errors and to present uniform language throughout.

Claims 1, 16 and 27 are amended. Claims 5 to 15 and 18 to 26 are canceled. New claims 30 to 36 are added. Claims 1, 16 and 27 are amended to distinguish over the references. Claim 1 is also amended in response to the rejection under 35 U.S.C. 112. New claims 30, 32 and 35 recite operation of this invention when the first fixed size is an integral multiple of the second fixed size as described in the application at page 38, line 20 to page 39, line 3. New claims 31, 33 and 36 recite operation of this invention when the first fixed size is not an integral multiple of the second fixed size as described in the application at page 39, lines 4 to 19 and illustrated in Figure 22A. New claim 34 recites subject matter recited in original claims 2 and 17 except dependent upon claim 27.

A new declaration by the sole inventor of this divisional application is attached.

Claim 1 was rejected under 35 U.S.C. 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The OFFICE ACTION states that claim 1 fails to recite "what entity is performing the step of receiving and arranging the data (step (c)) into second information blocks."

Claim 1 has been amended in response to this rejection. As amended claim 1 does not recite what entity performs any of the method steps. Step (a) now recites collecting emulation information "from" the data processor rather the prior "within" the data processor. The outputting step now no longer recites limitations related to the data processor. The Applicant regards the data

processor and the emulation circuits as separate entities. Independent apparatus claims 16 and 27 recite these as separate entities. Thus the Applicant believes that no method step recited in claim 1 is performed by the data processor. The language has been amended accordingly and the suggestion by the Examiner has not been adopted.

Additionally, the Applicant is aware of no general requirement that a method claim recite the entity that performs each method step. The Applicant believes this is permissive only, that is, the claim may recite an entity performing any or all method steps but is not required to do so. Accordingly, amended claim 1 is proper under 35 U.S.C. 112.

Claims 1 to 4, 8, 9, 15 to 17 and 27 were rejected under 35 U.S.C. 102(e) as being anticipated by Edwards, U.S. Patent No 6,732,307.

Claims 1, 16 and 27 recite subject matter not anticipated by Edwards. Claim 1 recites "arranging the collected emulation information into a plurality of first information blocks having a first fixed size." Claims 16 and 27 each recite a collector "collecting emulation information from said data processor and arranging said emulation information into a plurality of first information blocks having a first fixed size." Edwards fails to disclose this first fixed size. Edwards states at column 17, lines 45 to 48 (within the portion cited by the Examiner):

> "Trace buffer 901 may include either variable or fixed length messages, the largest size message entry 902 fitting within 3*64-bit words."

This disclosure of Edwards explicitly permits variable length messages and thus contradicts the recited first fixed size. Accordingly, claims 1, 16 and 27 are not anticipated by Edwards.

Claims 1, 16 and 27 recite further subject matter not anticipated by Edwards. Claim 1 recites "arranging the emulation information contained therein into a plurality of second information blocks having a second fixed size which differs from the first fixed size of the first information blocks." Claims 16 and 27 each recite an exporter "arranging said emulation information contained therein into a plurality of second information blocks having a second fixed size which differs from the first fixed size of said first information blocks." The OFFICE ACTION cites FIFO 202 as anticipating this subject matter. Edwards states at column 17, lines 21 to 24:

> "As discussed, FIFO 202 accepts one or more trace messages 801 which may be fixed size or variable length messages and provides these to trace buffer 227."

This portion of Edwards explicitly permits variable length messages. Additionally, the OFFICE ACTION points to no disclosure that FIFO 202 has a different length than trace buffer 901 as required by the above quoted limitations of claims 1, 16 and 27. The Applicant submits that Edwards includes no disclosure of this limitation. Accordingly, claims 1, 16 and 27 are not anticipated by Edwards.

Claims 1, 16 and 27 recite further subject matter not anticipated by Edwards. Claim 1 recites "outputting a sequence of the second information blocks via a plurality of terminals equal in number to said second fixed size." Claim 16 recites "a plurality of terminals for outputting information equal in number to said second fixed size" and the exporter is "for outputting a sequence of the second information blocks via said terminals." Claim 27 similarly recites the integrated circuits includes "a plurality of terminals coupled to said emulation controller equal in number to said second fixed size for outputting information to said emulation

controller, said exporter coupled to said terminals for outputting a sequence of said second information blocks to said emulation controller via said terminals." Edwards fails to disclose that the number of output terminals equals the number of bits in FIFO 202 as required by this language. Edwards includes no teaching regarding the number of terminals of transmission circuit 215 and thus cannot anticipate this subject matter. Accordingly, claims 1, 16 and 27 are not anticipated by Edwards.

Claims 2, 17 and 34 recite subject matter not anticipated by Edwards. Claims 27, 17 and 34 each recite "said second fixed size is smaller in size than said first fixed size." The OFFICE ACTION cites data compression disclosed at column 9, lined 55 to 60 of Edwards as anticipating this subject matter. The data compression disclosed in Edwards fails to anticipate the rearrangement of data from a first fixed size to a smaller second fixed size as recited in claims 2, 17 and 34. As taught in this application at page 38, line 16 to page 40, line 15, the rearrangement to a smaller fixed size in the second information blocks is independent of data compression. Thus this rearrangement can occur without data compression or may be used in conjunction with data compression. The data compression disclosure of Edwards fails to teach the second fixed size. Accordingly, claims 2, 17 and 34 are allowable over Edwards.

Claims 30, 32 and 35 recite subject matter not anticipated by Edwards. Claims 30, 32 and 35 recite "said first fixed size is an integral multiple of said second fixed size." This subject matter is not disclosed in Edwards. Claims 30, 32 and 35 further recite a manner of forming the second information blocks disclosed in this application at page 38, line 20 to page 39, line 3. This subject matter is not disclosed in Edwards.

Claims 31, 33 and 36 recite subject matter not anticipated by Edwards. Claims 31, 33 and 36 recite operation of this invention

when the first fixed size is not an integral multiple of the second fixed size as described in the application at page 39, lines 4 to 19 and illustrated in Figure 22A. In particular, Edwards fails to teach the recited current packet register and last packet register recited in these claims. Accordingly, claims 31, 33 and 36 are allowable over Edwards.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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